REMARKS

The Office Action of September 17, 2007 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1-11 were pending prior to the instant amendment. By this amendment, claim 1 is amended. Consequently, claims 1-11 are currently pending in the instant application.

Claims 1, 2 and 4-8 were rejected under 35 U.S.C. §102(b) as being anticipated by Yoneda et al. (U.S. Patent No. 5,726,942). Yoneda et al. however, fails to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claim 1 recites a combination that includes, among other things:

> controlling means for outputting transfer enable signals for controlling the blocking, transfer and latching of data transfer request signals to the data transfer request signal holding means based on the signals output from the prioritizing means.

At the very least, Yoneda et al. fails to disclose or suggest any of these exemplary features recited in the independent claim 1.

To establish anticipation under 35 U.S.C. § 102(b), the Examiner must show that each and every feature recited in these claims is either explicitly disclosed or "necessarily present" in a single prior art reference, such as within the four corners of the Yoneda et al. patent. *See* M.P.E.P.§ 2131(7th ed. 1998); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999); *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991). To support a conclusion of anticipation, the Examiner must specifically identify "substantial evidence" setting forth why and how the single prior art reference anticipates each and every feature recited in the claims. *See In re Mullin*, 481 F.2d 1333, 1336-37 (CCPA 1973) (An Examiner's bare assertion that claims were obviously anticipated by a reference did not

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inform the Applicant as to why the claims lacked novelty); *Dickinson v. Zurko*, 527, U.S. 150 (1999) (The U.S. Patent Office's findings of fact must be reviewed by the substantial evidence standard).

Viewed against this backdrop, each of the Examiner's factual conclusions must be supported by "substantial evidence" in the documentary record. See In re Lee, 61 U.S.P.Q.2d 1430, 1432 (Fed. Cir. 2002). The Examiner has the burden of documenting all findings of fact necessary to support a conclusion of anticipation or obviousness "less to 'haze of so-called expertise' acquire insulation from accountability." Id. To satisfy this burden, the Examiner must specifically identify where support is found within the prior art to meet the requirements of 35 U.S.C. §§ 102(b). In this case, however, the Examiner cannot satisfy his burden of demonstrating how Yoneda et al., taken alone or in combination with any other prior art reference, can either render obvious each and every one of the limitations present in independent claim 1 as required by the Manual of Patent Examining Procedure ("MPEP") and Federal Circuit jurisprudence.

The present invention is directed to an arbiter circuit as defined in amended claim 1 As discussed in Applicants' specification, the data transfer request signal holding means is controlled by the transfer enable signals (TRE/TREb) generated by the controlling means. The transfer enable signals control the blocking, transfer and latching of data transfer request signals. The controlling means is assigned to the gate circuit 23a and 23b in the disclosed embodiments. When one of the signals ARB_NO<1> is activated, signal TRE and TREb is switched to the "L" level and the "H" level, respectively. The transfer gates TR<0>-TR<2> block the inputs of the data transfer request signals ARBI<0>-ARBI<2>, and the holding circuits CINVO-CINV2 respectively latch the current status.

Yoneda et al. discusses a hierarchical encoder including timing and data detection devices for a content addressable memory. In reviewing the teachings of Yoneda et al. and

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particularly the encoder set forth therein, it is respectfully submitted that such a device fails to include or suggest a controlling means for outputting transfer enable signals for controlling the blocking, transfer and latching of data transfer request signals to the data transfer request signal holding means based on the signals output from the prioritizing means as is specifically recited by Applicants' claimed invention. Accordingly, it is respectfully submitted that independent claim 1 as well as those claims which depend therefrom clearly distinguishes over the teachings of Yoneda et al. and that such disclosure fails to include all the limitations presently set forth in independent claim 1. Therefore, it is respectfully submitted that independent claim 1 as well as those claims which depend therefrom are in proper condition for allowance.

Claims 3 and 9-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoneda et al. in view of Okabayashi et al. (JP 1993-259900). This rejection is respectfully traversed in that the publication to Okabayashi et al. fails to overcome the aforementioned shortcomings associated with the teachings of Yoneda et al. That is, while Okabayashi et al. may disclose a circuit comprising an even number of conduction resistors controlled CMOS inverters connected in a series, this reference fails to disclose or suggest that which is presently set forth by Applicants' claimed invention. Specifically, even if the teachings of Yoneda et al. are modified in the manner suggested by the Examiner in view of the teachings of Okabayashi et al., such combination fails to include or suggest an arbiter circuit including a data transfer request signal holding means, a prioritizing means for determining only a signal with the highest priority at a certain point as a valid signal and the signals with lower priorities as invalid signals in order to assign priorities to output signals from the data transfer request signal holding means, a controlling means for outputting transfer enable signals for controlling the blocking, transfer and latching of data transfer request signals to the data transfer request signal holding means based on the signals output from the prioritizing means

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and a delaying means for generating data transfer execution signals from the output signals of the prioritizing means as currently recited by Applicants' claimed invention. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 1 as well as claims 3 and 9-11 which depend therefrom, clearly distinguishes over the combination proposed by the Examiner and is in proper condition for allowance.

In view of the foregoing remarks, this claimed invention, as amended, is not rendered obvious in view of the prior art references cited against this application. Applicant therefore request the entry of this response, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Should the Examiner believe that a telephone conference would expedite issuance of the application, the Examiner is respectfully invited to telephone the undersigned patent agent at (202) 585-8316.

Respectfully submitted,

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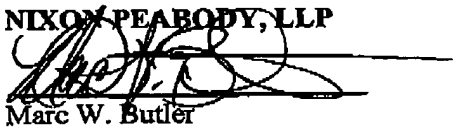

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